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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/548,826	04/13/2000	David E. Charlton	4076US(99-01860)	7750

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EXAMINER	
BRITT, CYNTHIA H	

ART UNIT	PAPER NUMBER
2138	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/548,826	CHARLTON ET AL.	
	Examiner	Art Unit	
	Cynthia Britt	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 1/23/06.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1,2,4-6,8,9,11,12,15 and 18 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1,2,4-6,8,9,11,12,15 and 18 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 6/14/04 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Arguments

Applicant's arguments filed January 26, 2006 have been fully considered but they are not persuasive.

As per applicant's argument:

"*Regarding claim 1, Applicants have amended claim 1 such that the at least one discrete non-volatile storage device is "configured for storing data indicating a location of at least one refurbishable failure associated with at least one of the plurality of discrete memory devices, wherein the at least one refurbishable failure comprises at least one failed output, and the at least one of the plurality of discrete memory devices is repaired or replaced-" With this amendment, Applicants assert that Dell et al. do not set forth each and every element of amended claim 1 as required for a 35 U.S.C j102 rejection.*

The added element of "wherein the at least one refurbishable failure comprises at least one failed output," was recited in claim 3. In rejecting claim 3, the Examiner states that "Dell et al. teach the memory module contains at least one failed output (column 3, lines 7-35, emphasis added)." However, this is not what claim 3, and now amended claim 1 recites. Amended claim 1 recites that the at least one refurbishable failure comprises at least one failed output and that the at least one refurbishable failure is associated with at least one of the plurality of discrete memory devices. Therefore, the failed output is an output of one of the discrete memory devices, not a failed output of the memory module.

Furthermore, Applicants assert that Dell et al. do not teach a failed output of one of the discrete memory devices as what is stored in the discrete non-volatile storage device. In the portion of the Dell et al. specification indicated in the Office Action, Dell et al. states that "the tag bits indicate . . . the 3-bit (one through eight binary) chip ID of the failing chip, i.e., which location on the SIMM has the bad data at the specified row address" (col. 3, lines 16-20). This portion of the specification does not indicate that an output of a memory device has failed. Rather, it indicates that a memory device has bad data at a specified row address. In addition, Applicants can find no disclosure of a failed output of one of the discrete memory devices anywhere in the Dell et al. reference."

The examiner would like to point out that a memory module is a memory device. The IEEE dictionary (along with other definitions) define a module as "A packaged functional hardware unit designed for use with other components." Or "The smallest component of physical management; i.e., a replacable device." Or "Multiple cells/units in a single assembly." As per applicant's argument that a failed output is not taught, in order to reference a failed address location, a failed output must have occurred at some point and therefore would be implied.

As per applicant's argument:

"*With respect to the second element added to amended claim 1, Applicants assert that Dell et al. do not teach that "the at least one of the plurality of discrete memory devices is repaired or replaced," as recited in amended claim 1. Claim 14 includes an element similar to this new element in claim 1. In rejecting claim 14, the Office Action states that "Dell et al. teaches repairing or replacing discrete memory*

devices on the memory module carrier substrate identified as having the at least one refurbishable failure (Figure 9E column 6 lines 40-49)." Applicants assert that this passage in Dell et al. does not disclose repairing or replacing discrete memory devices.

In other words, with respect to replacement, Dell et al. discloses replacing the ASIC, not the discrete memory devices. Applicants can find no reference in Dell et al. to replacing discrete memory devices on the module. With respect to repair, Dell et al. only state that the module is rejected for evaluation and possible rework may involve. In other words, it appears to Applicants that Dell et al. only teach possible rework of the module, not repairing discrete memory devices.

Furthermore, the process described in Dell et al. for avoiding failures in the memory devices is a process of remapping new memory locations to replace defective memory locations. Conversely, the present invention repairs or replaces the memory modules rather than remapping to avoid defective memory locations."

The examiner would like to point out that the quoted section states:

"If the fails are from address locations in the ASIC, the ASIC is identified for replacement in function block 118 and the module sent to repair. This could include re-mapping of the ASIC memory failures into alternate ASIC storage locations. If the fails exceed ASIC/EPROM storage limits, the module is rejected for evaluation and possible rework in function block 119 and the module sent to repair. If the fails are from non-remapped memory locations, the EPROM is re-written in function block 120 to add new address/chip failing locations. "

The examiner would like to point out that it is understood in the art that the act of remapping addresses that have failed is considered repair of the memory. As this is stated in the alternative, the replacement would not be required. However, Dell et al also teaches replacing or repairing a module figure 9E.

As the arguments for the other claims are substantially the same, the examiner will maintain the rejection as follows.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 2, 4-6 8, 9, 11, 12, 15 + 18 ~~1-19~~ rejected under 35 U.S.C. 102(e) as being anticipated by Dell et al. U.S. Patent No. 5,996,096.

As per claim 1, Dell et al. teach the claimed memory module (SIMM) having a memory module carrier substrate (printed circuit board), a plurality of discrete memory devices (DRAM chips) disposed on the memory module carrier substrate; and at least one discrete non-volatile storage device (EPROM) disposed on the memory module carrier substrate (column 2 lines 51-64), the discrete non-volatile storage device configured for storing data indicating a location of at least one refurbishable failure associated with at least one of the plurality of discrete memory devices (column 1 lines 47-52 failed memory locations, column 3 lines 15-20 chip ID/location column 3 lines 7-35 failed output, Figure 9E column 6 lines 40-49 repair or replace) .

As per claim 2, Dell et al. teach that the memory module uses a non-volatile storage device which is one of an EEPROM, an EPROM, or a flash memory chip (column 1 lines 47-52).

As per claim 4, Dell et al. teach the memory module in which a portion of the plurality of discrete memory devices are fully functional dice (Figure 9 A-B, column 6 lines 9-16). The examiner interprets the term 'fully functional dice' in the memory industry as one in which all 'bad' cells can be remapped or blocked from use.

As per claim 5, Dell et al. teach a computer system, having a processor (ASIC) and a memory module (SIMM) with a memory module carrier substrate (printed circuit board), a plurality of discrete memory devices (DRAM chips) disposed on the memory module carrier substrate and at least one discrete non-volatile storage device (EPROM) disposed on the memory module carrier substrate (column 2 lines 51-64), the at least one discrete non-volatile storage device configured for storing data indicating a location of at least one refurbishable failure associated with at least one of the plurality of discrete memory devices (column 1 lines 47-52 failed memory locations, column 3 lines 15-20 chip ID/location) .

As per claim 6, Dell et al. teach that the memory module uses a non-volatile

storage device which is one of an EEPROM, an EPROM, or a flash memory chip (column 1 lines 47-52).

As per claim 8, Dell et al. teach the memory module in which a portion of the plurality of discrete memory devices are fully functional dice (Figure 9 A-B, column 6 lines 9-16). The examiner interprets the term 'fully functional dice' in the memory industry as one in which all 'bad' cells can be remapped or blocked from use.

As per claim 9, Dell et al teach the testing of a memory module (Figure 9A-E). The memory module (SIMM) with a memory module carrier substrate (printed circuit board), a plurality of discrete memory devices (DRAM chips) disposed on the memory module carrier substrate and identifying data indicative of a location of at least one refurbishable failure associated with at least one of the plurality of discrete memory devices (column 6 lines 19-21); and storing the identified data (column 6 lines 21-24) on the memory module (column 1 lines 47-52 failed memory locations, column 3 lines 15-20 chip ID/location storing the identification of at least one failed output column 3 lines 7-35, column 6 lines 21-24, figure 9C-D) .

As per claim 11, Dell et al teach storing the identification of the failed output in the discrete non-volatile storage device on the memory module (column 6 lines 19-24 Figure 9C-D).

As per claim 12, Dell et el. teach that the memory module uses a non-volatile storage device which is one of an EEPROM, an EPROM, or a flash memory chip (column 1 lines 47-52, column 6 lines 19-24 Figure 9C-D).

As per claim 15, Dell et al teach a method of fabricating a memory module (SIMM) by placing a plurality of discrete memory devices (DRAM) on a memory module carrier substrate (printed circuit board), testing each of a plurality of elements associated with each of the plurality of discrete memory devices on the memory module carrier substrate and storing data indicative of a location of at least one discrete memory device including at least one element which failed a test. (Figures 9A-E column 6 lines 11-49) accessing the stored data indicative of the location of the at least one discrete memory device including the at least one element which failed the test (Figure 9D-E column 6 lines 31-36). at least one discrete memory device having the at least one failed element and repairing or replacing the at least one identified discrete memory device on the memory module substrate (Figure 9E column 6 lines 40-49).

As per claim 18, Dell et al teach testing the repaired or replaced discrete memory device on the memory module substrate (Figure 9E, column 6 lines 36-52).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

The examiner would like to invite applicant to call and discuss the language in the claims and in the prior art in order that more understandable claim language may be used or agreed upon to read over the prior arts and place this application in an allowable format.

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cynthia Britt whose telephone number is 571-272-3815. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 571-272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Cynthia Britt
Examiner
Art Unit 2138

EMMANUEL L. MOISE
SUPERVISORY PATENT EXAMINER